**Module 4: Amba3 Ahb-Lite Bus Architecture**

1. Which of the following tasks is NOT a function of the system bus?

1. Controlling the flow of data between processor and the memory block
2. Allowing information to be transferred between the processor and external peripherals
3. Connecting the ALU unit to the register file
4. Providing temporary buffer for control signals

2. Which of the following characteristics of an SoC is typically affected by the design of its bus?

1. Performance
2. Power consumption
3. Reliability
4. All of the above.

3. Why is there a need for communication standards?

1. To speed up the SoC design process
2. To improve SoC performance
3. To reduce SoC power consumption
4. All of the above.

4. Which of the following descriptions of Arm AMBA is incorrect?

1. AMBA is an open-standard, on-chip interconnect specification for the connection and management of functional blocks in SoC designs.
2. AMBA is one of the most widely used on-chip bus standard architectures.
3. AMBA is technology dependent.
4. AMBA promotes design reuse.

5. Which of the following AMBA bus families are used for low-bandwidth communication for peripherals access?

1. AXI
2. AHB
3. APB
4. ATB

6. Which of the following AMBA bus families would you use if you are designing a many-core SoC?

1. AXI
2. AHB
3. APB
4. ATB

7. Which of the following statements is incorrect?

1. AHB-Lite is a subset of AMBA AHB specification.
2. The AHB-Lite bus standard is typically used for multi-core processor systems.
3. AHB-Lite support can support multiple peripherals.
4. AHB-Lite is only suitable for SoCs with a single frequency.

8. What is the maximum number of AHB-Lite bus slaves that can receive data from a bus master simultaneously?

1. One
2. Ten
3. Three
4. The number is equal to the number of peripherals connected to the AHB-Lite bus.

9. Which of the following statements correctly describes the slave multiplexer in an AHB-Lite bus architecture? (There may be more than one correct answer.)

1. It is connected to all master blocks in the system.
2. It selects one of the slaves to receive data by decoding the address data available at its input.
3. It can temporarily buffer control signals during read transfer with a wait state.
4. The gate count of this block depends on the number of slaves in the system.

10. Which of the following statements is incorrect?

1. The data phase in the read transfer with wait state can last multiple clock cycles.
2. The address phase in the write transfer with wait state is only one clock cycle.
3. The address phase in the basic write transfer is only one clock cycle.
4. The data phase in the basic read transfer is only two clock cycles.